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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,510	08/27/2003	Fumitaka Arai	241987US2S	4228

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER
HO, TU TU V

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,510	ARAI ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) *8-23 and 25-39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

/

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/03 and 06/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 01/15/2004 is acceptable.

Election/ Restriction

2. Applicant's election with traverse of Species I, **claims 1-7 and 24**, in the reply filed on 09/20/2004 is acknowledged. The traversal is on the ground(s) that a search and examination of the entire application would not pose a serious burden. This is not found persuasive because Species I is directed to class 257, subclass 320, nonvolatile semiconductor memory device having floating gate on a substrate, and Species II, class 257, subclass 330, nonvolatile semiconductor memory device having floating gate in a trench in a substrate. Without a restriction requirement, a search and examination would not be thorough, and therefore would pose a serious burden.

The requirement is still deemed proper and is therefore made FINAL.

3. **Claim 8-23 and 25-39** are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 09/20/2004.

Drawings

4. **Figures 13 and 23 through 26** should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Fig. 4A, reference signs **2a and 2b**. In addition, the reference signs should be or are related to 2A and 2B respectively and should be accordingly described.

Specification

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 1 and 2** are rejected under 35 U.S.C. 102(b) as being anticipated by Park et al. U.S. Patent 5,736,443.

Park discloses in the figures and respective portions of the specification a nonvolatile semiconductor memory device as claimed.

Referring to **claim 1**, Park discloses a nonvolatile semiconductor memory device comprising:

a floating gate (13A, Fig. 2E) formed on a semiconductor substrate (11) via a gate insulating film (12);

diffused layers (15, 16), as sources or drain regions, which are positioned on opposite sides of the floating gate and which are formed in the semiconductor substrate;

first and second control gates (18A and 18B, column 3, lines 6-11) which are formed on the opposite sides of the floating gate and which drive the floating gate; and

an inter-gate insulating film (14) which insulates the first and second control gates (18A and 18B) from the floating gate (13A) and diffused layers (15 and 16).

Referring to **claim 2**, Park further discloses that the inter-gate insulating film (14) contacts opposite side walls of the floating gate and lower surfaces of the first and second control gates, and the first and second control gates are disposed opposite to the diffused layers.

8. **Claims 1-3, 6, and 24** are rejected under 35 U.S.C. 102(e) as being anticipated by Harari U.S. Patent Application Publication 2004/0165443.

Harari discloses in Figures 3-5 and 13 and respective portions of the specification a nonvolatile semiconductor memory device as claimed.

Referring to **claim 1**, Harari discloses a nonvolatile semiconductor memory device comprising:

a floating gate (34, Fig. 4) formed on a semiconductor substrate (the structure comprising layer 77) via a gate insulating film (91);

diffused layers (105, 106), as sources or drain regions, which are positioned on opposite sides of the floating gate and which are formed in the semiconductor substrate;

first and second control gates (82 and 83, paragraph [0040]) which are formed on the opposite sides of the floating gate and which drive the floating gate; and

an inter-gate insulating film (103/91, i.e., a film comprising a vertical portion, which is a vertical portion of film 103, and a horizontal portion, which is a stacked film of a horizontal portion of film 103 and a portion of film 91) which insulates the first and second control gates (82 and 83) from the floating gate (34) and diffused layers (105 and 106).

Note that "film" in inter-gate insulating (IGI) film is interpreted broadly. Specifically, "film" in the art is used to referred to either as a single-layer film or as a stacked film or a

layered film, as is evident by the use of "film" by Applicant to describe both a single-layer film (horizontal portion of IGI film) or a stacked film (vertical portion of the claimed IGI film).

Referring to **claim 2**, Harari further discloses that the inter-gate insulating film (103/91) contacts opposite side walls of the floating gate and lower surfaces of the first and second control gates, and the first and second control gates are disposed opposite to the diffused layers.

Referring to **claim 3**, Harari further discloses that the inter-gate insulating film includes first and second portions, the first portion (a vertical portion of 103) contacts the floating gate (34), the second portion (a horizontal portion 103 and a portion of 91) contacts the lower surface of the first or second control gate (82 or 83), and a thickness of the second portion (103/91) is larger than that of the first portion (103).

Referring to **claim 6**, Harari further discloses:

insulating materials (93 and 95, paragraphs [0041] through [0045], and Figs. 3 through 5B) which are formed on opposite side-surface sides disposed opposite to the diffused layers of the floating gate and which insulate adjacent memory cells;

first and second trenches (paragraph [0044]) formed in the insulating materials on the diffused layers; and

conductive materials (polysilicon, paragraph [0045]) which are formed in the first and second trenches to constitute the first and second control gates, wherein the first and second control gates of the adjacent memory cells are connected via the conductive materials (83, Figure 5B, in spatial relationship with Figs. 3 through 5A).

Referring to **claim 24**, and using the same reference numbers and citation as detailed above for claim 1, Harari discloses a nonvolatile semiconductor memory device comprising:

a floating gate formed above a semiconductor substrate;

first and second control gates which are formed on opposite sides of the floating gate and which are insulated from the floating gate and semiconductor substrate;

a first capacitance (CFS, Fig. 13) between the semiconductor substrate and floating gate;

a second capacitance (CCF1) between the first control gate and floating gate;

a third capacitance (CCF2) between the second control gate and floating gate;

a fourth capacitance (CCS1) between the first control gate and semiconductor substrate; and

a fifth capacitance (CCS2) between the second control gate and semiconductor substrate

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claims 4 and 7** are rejected under 35 U.S.C. §103(a) as being unpatentable over Harari in view of Dormans et al. U.S. Patent 6,326,661.

Referring to **claim 4**, Harari discloses a nonvolatile semiconductor memory device as claimed including IGI film 103/91 comprising the first portion 103 contacting the floating gate 34 and the second portion 103/91 contacting the lower surface of the control gate, just as detailed above. Harari further discloses that the first portion 103 is a stacked film including a silicon nitride film (ONO, paragraph [0044]) as claimed.

However, Harari fails to disclose that the second portion (103/91) is a silicon oxide film. Instead, Harari discloses that the second portion is a stacked film including silicon oxide film 91 (paragraph [0041]) and ONO film 103 including silicon oxide/silicon nitride/silicon oxide film.

Dormans, in disclosing a nonvolatile semiconductor memory device including IGI film 9 comprising a first portion contacting a floating gate 6 and a second portion contacting a lower surface of a control gate 7, discloses that the IGI film 9, the film that includes the first portion and the second portion, may comprise silicon oxynitride (SiON), or a sandwich of silicon oxide and silicon nitride (ONO), or silicon oxide (column 3, lines 40-43 and column 4, lines 36-42), thereby teaching that the various materials and layer format (i.e., as single layer or stacked layer) for IGI films are art equivalents.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the second portion of Harari's IGI film 103/91, and noting that 91 is already formed of silicon oxide, using silicon oxide. One would have been motivated to make such a modification in view of the teachings of Dormans that the mentioned various materials and layer format for the second portion of the IGI films are art equivalents.

Regarding **claim 7**, the device of Harari, modified in view of Dormans just as detailed, further comprises:

a third trench (100, Harari, Fig. 5A and 5B) which is formed opposite to a side surface different from that in contact with the first and second control gates of the floating gate (Figs. 5A and 5B, in spatial relationship with Figs. 3 and 4); and

a second insulating material (thick oxide layer to form STI, paragraph [0042]) embedded in the third trench,

wherein bottom surfaces of the first and second control gates (no individual label, portions collectively referred to as 83 in Fig. 5B) on the second insulating material in the third trench (100) are higher than those of the first and second control gates on the semiconductor substrate (Fig. 5B, in spatial relationship with Figs. 3 and 4).

10. **Claim 5** is rejected under 35 U.S.C. §103(a) as being unpatentable over Harari in view of Dormans, as detailed above, and further in view of Wils et al. U.S. Patent 6,642,103.

As mentioned above, Harari and Dormans disclose a nonvolatile semiconductor memory device wherein the first portion is a single layer or stacked film containing silicon oxide or silicon nitride, and the second portion is a silicon oxide film. However, the references fail to disclose that the first portion contains aluminum oxide. Wils, in disclosing a nonvolatile semiconductor memory device comprising a floating gate, an IGI film, and a control gate, teaches that the IGI film may be composed of silicon oxide, tantalum oxide, aluminum oxide, silicon nitride, silicon oxynitride (SiON), or ONO (column 4, lines 50-60), thereby teaching that the various materials are all suitable for IGI films. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first portion of the Harari-Dormans' device containing aluminum oxide. One would have been motivated to make such a modification in view of the teachings by Wils that such a material one of ordinary skill in the art would use for forming IGI films.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
September 29, 2004